REMARKS

Previous claims 1 and 4 to 9 are being canceled from this application and are being replaced by new claims 63-84.

The Examiner has rejected previous claims 6 to 9 under 35 U.S.C. §101, as claiming the same invention as that of claims 1 to 4 of prior U.S. Patent No. 5,418,752.

The double patenting rejection is believed improper as the previous claims are not duplicates of the claims of prior U.S. Patent No. 5,418,752. In any case, this rejection is now moot, as new claims 63 to 80 are replacing the previous claims.

New claims 63 to 84, while directed to the same subject matter of the invention claimed in U.S. Patent No. 5,418,752, are believed not duplicative of the claims therein.

The Examiner has rejected previous claims 1, 4 and 5 under 35 U.S.C. §103 as being unpatentable over Ali et al. or Sparks et al in view of Rao.

New independent claims 63, 70, 74 and 80 include features of multiple sector erasure that are not taught or suggested by the references of record. For example, each sector storing multiple bytes of data is addressable for erasure and different combinations of multiple sectors are selectable for erasure.

Ali et al., discloses an interface circuit between a host and a plurality of flash EEPROM chips. There is no disclosure of partitioning each chip into a plurality of erasable sectors. Furthermore, while more than one chip are shown sharing a common bus, only one chip can be selected at a time to communicate with the bus, as each is conventionally enabled by a chip select signal 68. Even if the chip could be argued to constitute a sector, there is no possibility of erasing more than a single chip at a time.

Sparks et al., disclose splitting the EEPROM array into two or more subarrays. Each subarray is physically separate and independent and has its own data and address bus. The motivation is to allow independent operation in the two subarrays, e.g., "in allowing one part of the EEPORM to be programmed while the program stored in another part of the EEPROM or RAM may be read and

utilized." "Erasing is performed on all bytes within a single array, or on all arrays at once, as in a bulk erase." (Col. 3, lines 44-46.) This only allows for the possibility of selecting either one or all of arrays for erasure.

Rao discloses an EEPROM with an architecture that supports erasure in either a flash erase mode or a byte erase mode. In other words, either the whole chip is flash erased or a byte (8 bits) of memory is erased. There is no disclosure or suggestion of multiple sectors erase as in the claimed invention.

Thus, Ali et al., Sparks et al. and Rao, individually or in combination, do not allow for the possibility of multiple sector erase as recited in independent claims 63, 70, 74 and 80 and all claims dependent thereon.

A number of references that have recently come to the attention of the undersigned are being disclosed in an Information Disclosure Statement with accompanying PTO Form 1449 filed herewith. Reviewing of the references and making them of records by the Examiner is respectfully requested.

Claims 63 to 84 are now pending. Reconsideration of the rejection is respectfully requested in view of the amendment and explanations.

Respectfully submitted,

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